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MICROPROCESSOR UNIT FOR EXPERIMENTAL PROCESS DATA*

by

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I. INTRODUCTION

Microprocessor application to data acquisition system control establishes a novel approach to monitoring processes utilizing test equipments with diverse output characteristics. This microprocessor data acquisition system generates a hard copy for immediate data observation and stores data on a magnetic tape cassette for subsequent transmission to central computing facilities for statistical evaluations.

The program software requires 3300 Programmable Read Only Memory 8-bit locations and 100 Random Access Memory 8-bit word locations. Input data and output control software interfaces are implemented with programmed I/O. The printer/magnetic tape cassette terminal and real time generator software interfaces are implemented with priority interrupt. The PL/M high level programming language has been utilized to realize the microprocessor programming requirements.

The experimental process monitored is characterized by one electrical analog output signal. This signal contains two parameters for which data must be accumulated. The RMS value of the sin wave magnitude is measured by an analog to digital converter in a 4 1/2 digit digital multimeter. The period of the sin wave is measured by a frequency to period converter in a 7 digit

* Work performed under the auspices of the USERDA.

digital counter.

The diverse output characteristics of the test equipment presents challenging software and hardware interface design. The digital interface logic polarity and timing requirements encountered are representative of the diverse signals common to data acquisition systems. The digital multimeter outputs five byte-serial characters of parallel data consisting of the binary coded decimal numeric value and character status information. The output sequence cycles from least significant to most significant character. The presence of a character is indicated by a 1μs active low pulse. The status information identifies the decimal point location and the least significant character. The A/D conversion cycle is 1.25ms.

The digital counter outputs seven byte-serial characters of parallel binary coded decimal numeric value. The output sequence cycles from most significant to least significant character with an eighth output separating the most significant from the least significant character. Valid updated output data is available approximately 100μs after a 1μs active high output pulse. The presence of a character is indicated by a 150μs active high pulse. The F/D conversion cycle varies from 0.1 to 2.5 seconds as a function of the signal period. Decimal point information is not available as an output signal.

The microprocessor in the data acquisition system initiates data conversion program cycles for five second interval measurements, organizes input character sequences, calculates data averages every 50 seconds and directs input/output control. In addition, the microprocessor adds intelligence to the magnetic tape terminal by sequencing and maintaining initial control instructions to be followed by the operator. The microprocessor enhances the

data acquisition by manipulating operator inputs which add variable data identifiers such as date, process sequence and test equipment switch setting information. Measurement instrument switch setting information is required for proper decimal point determination.

II. DATA ACQUISITION CONFIGURATION

The microprocessor hardware system is implemented with the Intel 8080 Microprocessor. The 8080 MPU is an 8-bit parallel central processing unit. The MPU is fabricated on a single LSI chip utilizing n-channel silicon MOS technology. The instruction cycle time is 2μs as a function of the externally implemented 2-phase clock.

MPU architecture consists of six 8-bit data registers, an 8-bit accumulator, four 8-bit temporary registers, four testable flag bits and an 8-bit parallel binary arithmetic unit. Decimal arithmetic capability is utilized in this system to eliminate input data BCD to binary conversion before the averaging calculations and correspondingly to eliminate binary to BCD conversion prior to output printing by the data terminal.

Multiple level interrupt capability is available with the MPU when the hardware includes sufficient Random Addressable Memory to allow stack storage. The MPU contains a 16-bit stack pointer. The stack architecture allows any portion of RAM to be used as a last-in/first-out stack to store and reload the contents of the accumulator, the 4 flag bits, or any of the data registers.

The MPU System architecture of this Data Acquisition System is shown in Figure #1. The MPU block contains the Intel 8080 MPU, the 2-phase clock generator and driver, address bus buffers, bi-directional data bus buffers,

control line buffers, status information register, and priority interrupt manager.

The 2-phase clock is derived from a 16MHz crystal oscillator. A National Semiconductor TTL MSI counter DM8563 divides the 16MHz clock to obtain 8, 4, 2 and 1MHz. Combinational Texas Instruments Schottky TTL logic generates the 2MHz 2-phase clock frequency. Level translation by Fairchild 9607 Quad Bipolar-to-MOS Level Shifter and Driver is required to drive the MPU. All other MPU input/output signals are TTL levels.

The TTL 2MHz 2-phase clocks required for ROM, RAM, and Serial I/O logic timing are buffered by Signetics 8T95 High Speed Hex Tri-State Buffers. The 16-bit address bus is driven by 2 and 4/6 dual-in-line packages of the 8T95 Tri-State Buffers. A similar device, the Signetics 8T96 Inverting High Speed Hex Tri-State Buffer, provides the buffered control lines. Two Intel 8216 4-bit Parallel Bi-Directional Bus Drivers interface the MPU to the 8-bit data bus.

Instructions for the 8080 MPU require from one to five machine cycles for complete execution. The MPU sends out 8 bits of status information on the data bus at the beginning of each machine cycle. These 8 bits are latched for I/O control requirements by an Intel 8212 8-bit Input/Output Port.

Eight levels of priority interrupts are provided by the Intel 8214 Priority Interrupt Control Unit. Software output instructions enable and mask lower level interrupts. An enabled interrupt vectors the program counter to location ØØXXXØØØ where XXX is the binary value of the active interrupt level.

The MPU system provides 256 words of 8 bits of RAM. The two random access memory devices are Signetics 2606-1 256 words by 4 bits Random Access Read/Write Static Memory. One RAM provides the upper four bits with the second RAM providing the lower four bits. The software instructions are stored in fourteen Intel 1702A, 2048 bit Erasable and Electrically Programmable Read Only Memory which contain 256 eight-bit words each. The PROM(s) provide the advantage of non-volatile memory and the advantage of ultraviolet light erasure for software updating without additional hardware cost.

The real-time clock generator provided is controlled by software control to establish 2MHz clock divide by N MSI logic to generate an interrupt. A real time clock of period P is then obtained by summing the corresponding number of interrupts. The data acquisition system program commands an 0.5 second interrupt. Three and five second periods are realized by summing 6 and 10 interrupts respectively.

The data terminal interface standard is RS-232C. A General Instruments AY-5-1013 UART Universal Asynchronous Receiver Transmitter LSI device provides the serial I/O logic interface. The LSI subsystem device generates an interrupt after each input ASCII character. The UART is fully double buffered to eliminate the need for system synchronization.

The LSI device also provides outputs for parity error, data over-run (a new input character present before old character has been read) and framing error which indicates that a stop bit was not received. The UART output circuitry is Tri-State to interface with the data bus structure. The transmitter output line is driven by a Motorola MC 1488L Quad Line Driver special purpose circuit. The transmitter output conforms to EIA Standard RS-232C. The receiver input line driver is a Motorola MC 1489L Quad Line Receiver

special purpose circuit. The line receiver also conforms to RS-232C. The data acquisition system serial data transmission rate is 300 Baud.

The interfaces to the Digital Counter and Digital Multimeter are controlled by the Intel 8212 8-bit Input/Output Port. Input ports Ø, 1, 2 and output port 1 are I/O ports. The Intel 8212 port consists of an 8-bit latch with Tri-State output buffers along with control and device selection logic.

Handshaking features are provided by an internal 8212 Service Request flip-flop for identification of port status to the MPU and I/O devices. Input ports Ø and 1 accept measurement data. Output port 1 provides the start of conversion control for program synchronization. Input port 2 provides an end of frequency to period conversion signal to the MPU.

The Service Request outputs of the three input ports are provided to the MPU 8-bit data bus by input port 3 which is a Signetic 8T95 Tri-State Buffer. Only a buffer is needed since the signal is latched in the I/O port devices. The Service Request flip-flop active low output (set state) identifies that an input has occurred. When the MPU reads the input, the Service Request flip-flop is cleared to the high state (cleared state).

III. MEASUREMENT INSTRUMENT INTERFACES

Interaction of the MPU and the measurement instruments present the most challenging system design problems. The instruments are similar in design concept in that each instrument has two functional sections. One section of each instrument conditions the input signal and converts it to Binary Coded Decimal digital data.

The second section contains the data storage latches, Light Emitting Diode display, and LED and output multiplexing control. The data storage latches are updated after an input conversion. The data is then multiplexed

to the LED displays and external output sequentially by character at a much higher rate than the input conversion rate. To examine the interaction of the MPU and the measurement instruments, specific I/O signals of the Digital Multimeter and Digital Counter must be identified. The I/O signals available are diverse and must be considered separately.

IV. INPUT-OUTPUT REQUIREMENTS - DIGITAL COUNTER

The Digital Counter outputs seven parallel characters byte-serial starting with the most significant to the least significant characters. An additional or eighth sequence slot is inserted to allow internal updating and reading synchronization. Figures 2 and 3 Timing Diagram illustrate the output timing of the signals.

The measurement timing is totally asynchronous to the output display multiplex timing. Figure 2 illustrates the measurement timing where the Data Good or latch signal indicates the end of conversation. The trailing edge of the Data Good signal sets the port 2 Service Request flip-flop output. However, the output data valid condition is not actually present until approximately 100μs after the Data Good signal. The output data valid condition is not an output signal. Therefore, the MPU software must generate the 100μs delay. The MPU reads the input port 3 to examine input port 2 Service Request flip-flop.

Upon detecting the Service Request flip-flop set condition, the MPU reads input port 2 to clear the Service Request flip-flop. Then input port 3 is read to examine the Service Request flip-flop of input port 1.

Input port 1 data is loaded and Service Request flip-flop is set by a signal derived from the output section SCAN CLOCK shown in Figure #3. The

derived signal is a single shot signal triggered by the trailing edge of SCAN CLOCK. The data and TSØ signals are not stable until after the leading edge of SCAN CLOCK. Therefore, initially the trailing edge of SCAN CLOCK was used to load port 1. However, the MPU examination of the Service Request flip-flop is asynchronous to the SCAN CLOCK. Data is gated through the port when the load signal is active high and an input instruction is being executed. Therefore, by the time the MPU has read the port from the least significant character LSC SCAN CLOCK, the time slot Ø TSØ signal could be active. This condition could initiate the MPU software input sequence resulting with a question mark (all data lines high) in the most significant character position and the actual data right-shifted one character position.

By including the SCAN CLOCK as an additional data bit and examining it for the low state, the ambiguity is avoided since TSØ starts changing on the leading edge of the SCAN CLOCK. The narrow pulse used to load input port 1 allows SCAN CLOCK to go low before loading the data.

In summary of the Digital Counter I/O Requirements, the timing of the available signals requires hardware altering to achieve stable data inputs. In addition, software timing delays are required to compensate for signals not present in the output.

V. INPUT/OUTPUT REQUIREMENTS - DIGITAL MULTIMETER

The Digital Multimeter outputs five parallel characters byte-serial starting with the least significant character. A data bit is included to identify the LSC. A SCAN CLOCK is included to synchronize the reading. Figures 4 and 5 illustrate the Digital Multimeter timing diagrams.

One data bit DATA GOOD is included in the output to identify the valid

data condition. Figure 4 defines the timing of the signal. The analog to digital conversion time is fixed; therefore, the output is correspondingly available at fixed times only. This relationship eliminates the end of conversion complexity experienced with the Digital Counter. The DATA GOOD line is synchronized to the output timing as shown in Figure 5. The DATA GOOD line goes active high immediately after the LSC slot.

The data is stable at all times while the SCAN CLOCK line is high. Data changes during the 1μs low period of SCAN CLOCK. Input port Ø is loaded with a signal derived from the leading edge of SCAN CLOCK.

In summary of the Digital Multimeter I/O requirements, the timing of the available signals requires hardware altering to achieve stable data inputs for the type input port device used. All signals necessary to define the data including a decimal point are contained in the corresponding character sequence output.

VI. INPUT/OUTPUT REQUIREMENTS - TERMINAL

The data terminal interface is EIA Standard RS-232C. Therefore, no special considerations are required. The UART generates an interrupt when a character is received. The interrupt steals the MPU program control, inputs the character and returns the MPU program control.

VII. SOFTWARE IMPLEMENTATION

The software programming was achieved using Intel's PL/M 8080 high level Programming Language. The PL/M program is a sequence of "declarations" and "executable statements" as opposed to an assembly language program which is a sequence of machine language instructions. The PL/M compiler was used to translate the PL/M language to machine language. Pass 1, PLM 1, is exe-

cuted first with the saved PL/M program as an input. Diagnostic messages may result which require PL/M program corrections. PASS 2, PLM2, generates the machine language code. The machine language may also be generated by the Intel 8080 assembler that translates the assembly language (operation code mnemonics) to machine language.

The software program was simulated by the use of a FORTRAN IV program Intel INTERP/80. The INTERP/80 accepts machine code produced by the Intel PL/M 80 compiler or the Intel 8080 assembler. The simulator requires execution commands to exercise the program.

The machine language is in the form of BNPF data streams where B identifies the start of an eight bit word, N identifies a logic "0", P identifies a logic "1", and F identifies the end of an eight bit word. The BNPF data streams are loaded into MPU memory PROM(s) then executed.

VIII. SOFTWARE PROGRAM

The Data Acquisition System software program combines data collection, data averaging, and data terminal control. The MPU stores the assembled and averaged data on the data terminal magnetic tape cassette. The tape is loaded with ASCII coded characters for subsequent transmission to central computing facilities for subsequent statistical evaluations.

The software program is interactive with the process operator through the data terminal keyboard. The software allows for terminal real time factors such as carriage return time. The MPU outputs initialization instructions on the printer to guide the operator in properly loading the magnetic tape cassette and setting the proper recording switch commands. After each output message to the operator, the MPU waits for an operator keyed carriage return.

The MPU software program then requests the data terminal status through remote control commands to verify that the correct switch settings have been executed by the operator. An error message is printed out when the operator has not completed instructions correctly.

Upon completion of data terminal initialization, the MPU program requests the operator to identify switch position settings on the Digital Counter and Digital Multimeter. The MPU can only test the operator input since no electrical signals of the switch positions are available.

Data and process dependent information is then requested. The process dependent information relates to test number of process cycle number. The data acquisition system is now initialized and ready for the operator to type a line feed command to start the data acquisition.

The software data acquisition program starts the frequency to period conversion in the Digital Counter. A three second wait loop is initialized to allow for the variable conversion time. A five second time loop is initialized to achieve an update measurement every five seconds.

The Digital Multimeter input port Service Request flip-flop is examined by reading Input Port 3. When a character has been loaded, the MPU reads the data available in Input Port Ø. A test is made to verify valid data and least significant character identification. The program loops until the test is satisfied. The five characters are then collected and assembled for output and averaging.

The Digital Counter Data Good Service Request flip-flop (Input Port 2) is examined after three seconds for the end of conversion condition. When this condition is satisfied, the MPU clears Input Port 2 and begins to ex-

amine Input Port 3 for an Input Port 1 service request flip-flop condition. Input to Port 2 results in a software test for time slot zero and the low state of the Input SCAN CLOCK. The program loops until the test is satisfied. The next seven inputs to Input Port Ø are then collected and assembled for output and averaging.

The program outputs both instrument readings in one line of print and one half block of cassette data to the data terminal. The program idles until the 5 second loop is realized and then begins again. Every tenth program cycle results in the averaging of the corresponding ten input readings. The Intel 8080 BCD arithmetic capability with the Decimal Adjust instruction allows averaging without BCD to binary and then binary to BCD conversion.

The program allows data collection and storage of 256 blocks of 50 seconds of data. Therefore, the data acquisition system will automatically terminate a run after approximately 3 1/2 hours. The operator may key a termination at any time which will result in a termination at the end of the present 50 second block and print out of re-start instructions.

IX. MPU SYSTEM CHECKOUT

Incorporation of the software program machine language into a checkout Random Access Memory is accomplished by utilizing the data terminal cassette playback capability. The BNPF format is copied on to the cassette from the central computing facility over a 300 baud line.

The checkout of the system with new machine language and new hardware was accomplished with state-of-the-art digital data domain test equipment. The mapping function of the Hewlett Packard 1600/1607A Logic State Analyzer system graphically displays the active program addresses and provides a cursor controlled by data polarity switches to isolate the address of undesirable pro-

gram loops. The data domain equipment also allows address and data bit correlation to isolate checkout difficulties. The machine language is converted to firmware for final system configuration. The BNPF format is used to program the Intel 1702A Erasable and Electrically Programmable Read Only Memory devices.

X. SUMMARY

Microprocessor application to data acquisition system control established a novel approach to monitoring processes utilizing test equipment with diverse output characteristics. This microprocessor system data acquisition system generates, every five seconds, a hard copy for immediate data observation and stores data on magnetic tape cassette for subsequent transmission to central computing facilities for statistical evaluation. The program requires approximately 3300 program storage memory locations and 100 temporary storage locations to complete the data acquisition requirement for this experimental process.

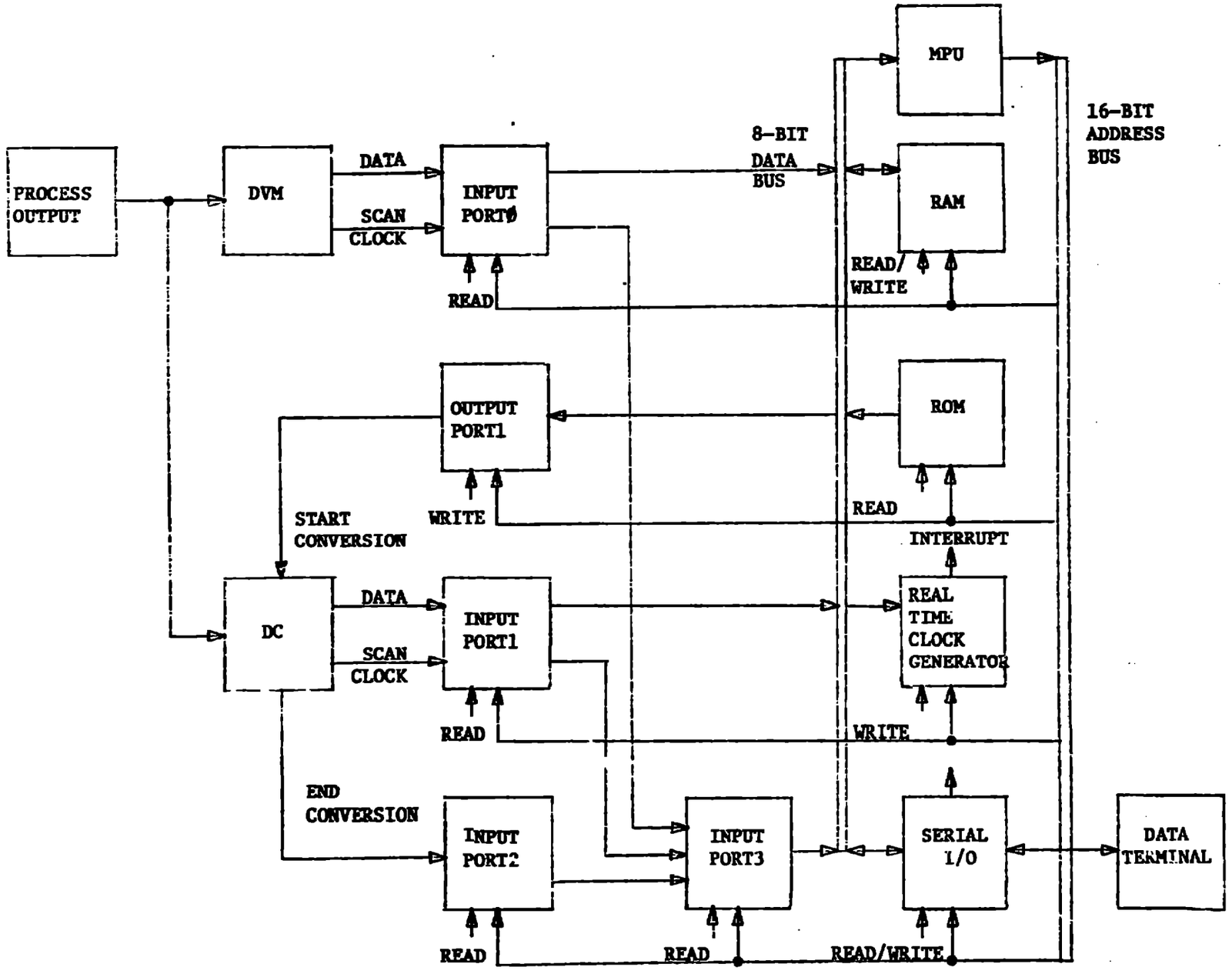

FIGURE 1. MPU SYSTEM ARCHITECTURE

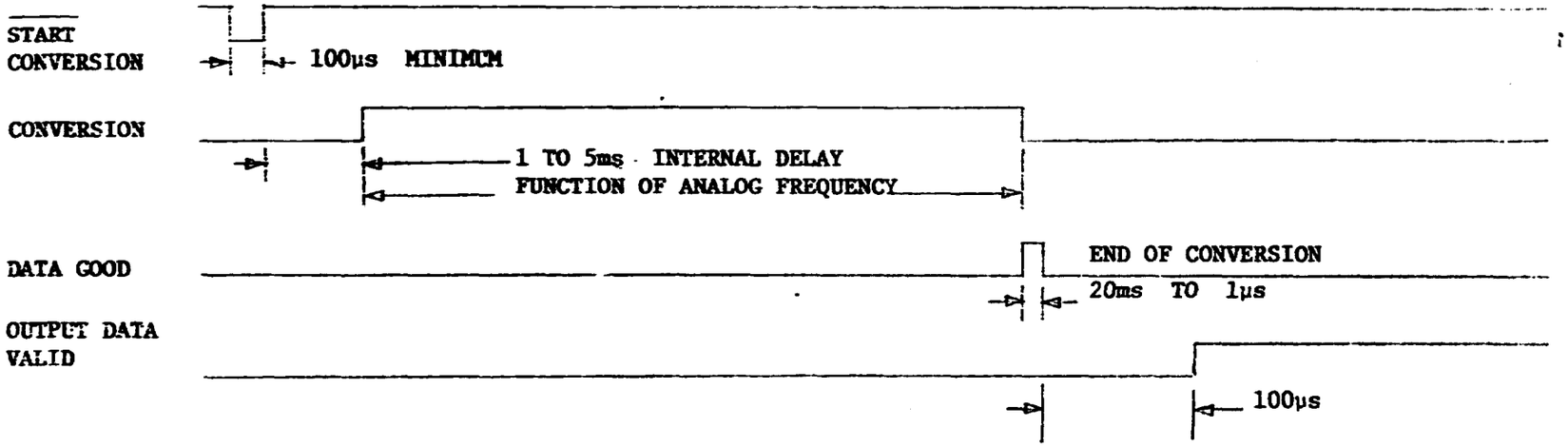

FIGURE 2. DIGITAL COUNTER MEASUREMENT TIMING DIAGRAM

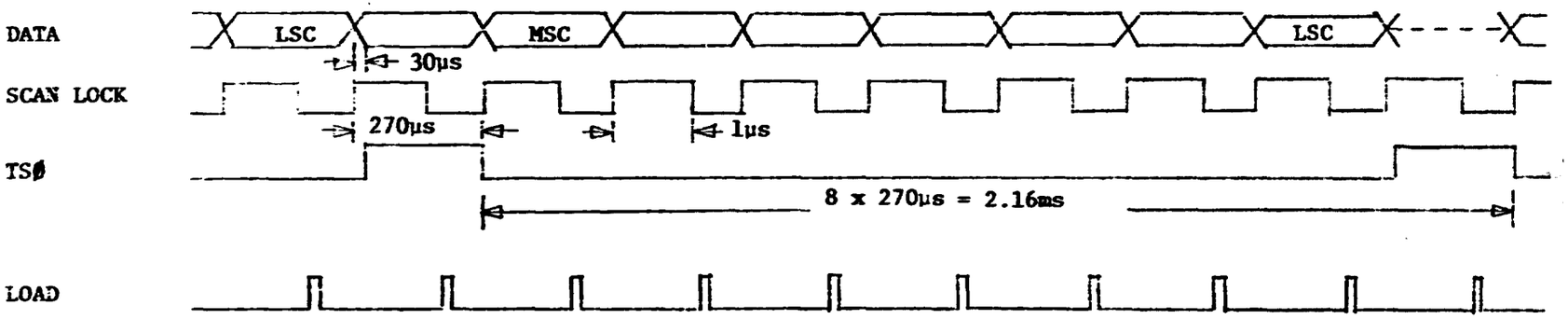

FIGURE 3. DIGITAL COUNTER OUTPUT TIMING DIAGRAM

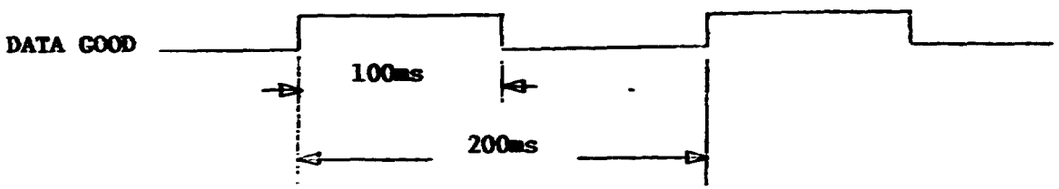

FIGURE 4. DIGITAL MULTIMETER MEASUREMENT TIMING DIAGRAM

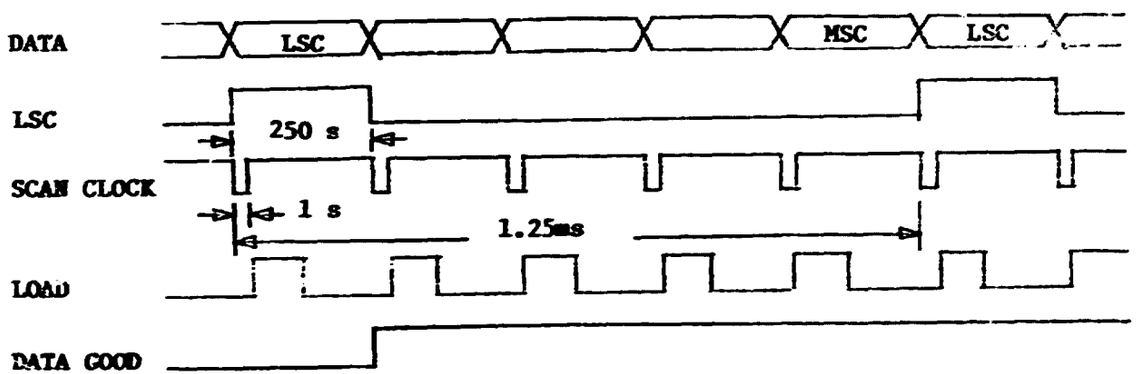

FIGURE 5. DIGITAL MULTIMETER OUTPUT TIMING DIAGRAM